

# Design of Unified Power Quality Conditioner for power quality problems

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## ABSTRACT

This paper introduces a new concept of optimal utilization of a unified power quality conditioner (UPQC). The series inverter of UPQC is controlled to perform simultaneous 1) voltage sag/swell compensation and 2) load reactive power sharing with the shunt inverter. The active power control approach is used to compensate voltage sag/swell and is integrated with theory of power angle control (PAC) of UPQC to coordinate the load reactive power between the two inverters. Since the series inverter simultaneously delivers active and reactive powers, this concept is named as UPQC. A detailed mathematical analysis, to extend the Power Angle Control PAC approach for UPQC, is presented in this paper. MATLAB R2013a/SIMULINK-based simulation results are discussed to support the developed concept. Finally, the proposed concept is validated with experimental study.

**Keywords:** Active power filter (APF), power angle control (PAC), power quality, unified power quality conditioner (UPQC), voltage sag and swell.

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## I. INTRODUCTION

With the advent of power semiconductor switching devices, like thyristors, GTO's (Gate Turn off thyristors), IGBT's (Insulated Gate Bipolar Transistors) and many more devices, control of electric power has become a reality. Such power electronic controllers are widely used to feed electric power to electrical loads, such as adjustable speed drives (ASD's), furnaces, computer power supplies, HVDC systems etc[1]-[5]. The power electronic devices due to their inherent non-linearity draw harmonic and reactive power from the supply. In three phase systems, they could also cause unbalance and draw excessive neutral currents. The injected harmonics, reactive power burden, unbalance, and excessive neutral currents cause low system efficiency and poor power factor. In addition to this, the power system is subjected to various transients like voltage sags, swells, flickers etc. These transients would affect the voltage at distribution levels. Excessive reactive power of loads would increase the generating capacity of generating stations and increase the transmission losses in lines. Hence supply of reactive power at the load ends becomes essential. Power Quality (PQ) has become an important issue since many loads at various distribution ends like adjustable speed drives, process industries, printers, domestic utilities, computers, microprocessor based equipments etc. have become intolerant to voltage fluctuations, harmonic content and interruptions. In this paper, a UPQC topology with reduced dc-link voltage is proposed. The topology consists of capacitor in series with the interfacing inductor of the shunt active filter. The series capacitor enables reduction in dc-link voltage requirement of the shunt active filter and simultaneously

compensating the reactive power required by the load, so as to maintain unity power factor, without compromising its performance. This allows us to match the dc-link voltage requirements of the series and shunt active filters with a common dc-link capacitor. Further, in this topology, the system neutral is connected to the negative terminal of the dc bus[5]. This will avoid the requirement of the fourth leg in VSI of the shunt active filter and enables independent control of each leg of the shunt VSI with single dc capacitor. The simulation studies are carried out using Matlab/Simulink R2013a simulator, and detailed results are presented in the paper. A prototype of three-phase UPQC is developed in the laboratory to verify the proposed concept, and the detailed results using 435 II PQ Analyzer are presented in this paper.

## II. UNIFIED POWER QUALITY CONDITIONER (UPQC)

A Distributed Static Compensator (DSTATCOM) is a voltage source inverter based static compensator shown in Fig.1 that is used for the correction of bus voltage sags. Connection (shunt) to the distribution network is via a standard power distribution transformer. The DSTATCOM is capable of generating continuously variable inductive or capacitive shunt compensation at a level up to its maximum MVA rating. The DSTATCOM continuously checks the line waveform with respect to a reference ac signal, and therefore, it can provide the correct amount of leading or lagging reactive current compensation to reduce the amount of voltage fluctuations.

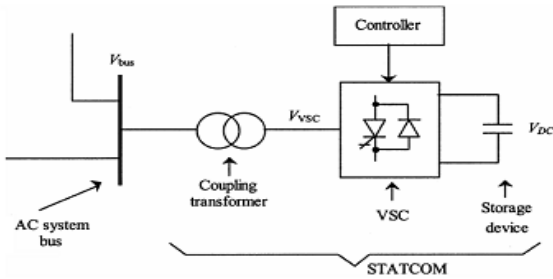


Fig.1. Schematic representation of the DSTATCOM

**B. Dynamic Voltage Restorer (DVR).**

The DVR mitigates voltage sags by injecting a compensating voltage into the power system in synchronous real time. The DVR is a high-speed switching power electronic converter that consists of an energy storage system that feeds three independent single-phase pulse width modulated (PWM) inverters. As shown in Fig. 2 the energy storage system for the DVR is a dc capacitor bank, which is interfaced to the PWM inverters by using a boost converter (dc to dc). The boost converter regulates the voltage across the dc link capacitor that serves as a common voltage source for the PWM inverters. The three voltage source single-phase PWM inverters (dc to ac) synthesize the appropriate voltage waveform as determined by the DVR's digital control system. This compensating voltage waveform is injected into the power system through three single-phase series injection transformers. The DVR control system compares the input voltage to an adaptive reference signal and injects voltage so that the output voltage remains within specifications.

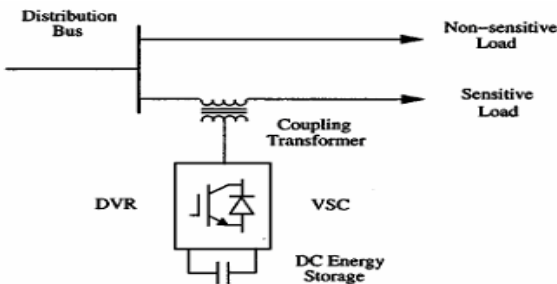


Fig.2 . Schematic representation of the DVR1

**C. Unified Power Quality Conditioner (UPQC)**

The Unified Power Quality Conditioner (UPQC) is a more complete solution for the power quality problem. The basic structure of this equipment is shown in shown in Fig 3. In this figure, the UPQC is an association of a series and shunt active filter based on two converters with common dc link. The series converter has the function to compensate for the harmonic components (Including unbalances) present in the source voltages in such a way that the voltage on the load is sinusoidal and balanced.

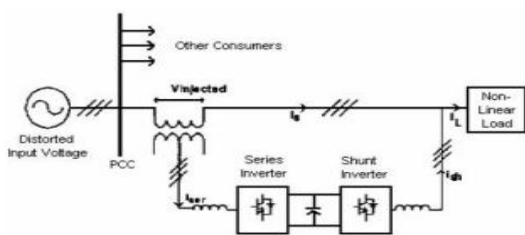


Fig .3. Basic Block Diagram of UPQC

The shunt active filter has the function of eliminating the harmonic components of nonlinear loads in such a way that the source current is sinusoidal and balanced. This equipment is a good solution for the case when the voltage source presents distortion and a harmonic sensitive load is close to a nonlinear load as shown in Fig 4. To provide a balance, distortion-free, and constant magnitude power to sensitive load and, at the same time, to restrict the harmonic, unbalance, and reactive power demanded by the load and hence to make the overall power distribution system more healthy, the unified power quality conditioner(UPQC) is one of the best solutions. A unified power quality conditioner (UPQC) is a device that is similar in construction to a unified power flow conditioner (UPFC). The UPQC, like a UPFC, employs two voltage source inverters (VSIs) that are connected to a common dc energy storage capacitor. One of these two VSIs is connected in series with the ac line while the other is connected in the shunt with the same line. A UPFC is employed in a power transmission system to perform shunt and series compensation at the same time. Similarly a UPQC can also perform both the tasks in a power distribution system. A power distribution system, on the other hand, may contain unbalance, distortion and even dc components. Therefore a UPQC must operate under this environment while providing shunt or series compensation. Generally, a 3P4W distribution system is realized by providing a neutral conductor along with three power conductors from generation station or by utilizing a three-phase  $\Delta$ -Y transformer at distribution level. A 3P4W distribution network considering, a  $\Delta$ -Y transformer. Assume a plant site where three-phase three wire UPQC is already installed to protect a sensitive load and to restrict any entry of distortion from load side toward utility. If we want to upgrade the system now from 3P3W to 3P4W due to installation of some single-phase loads and if the distribution transformer is close to the plant under consideration, utility would provide the neutral conductor from this transformer without major cost involvement. In certain cases, this may be a costly solution because the distribution transformer may not be situated in close vicinity.

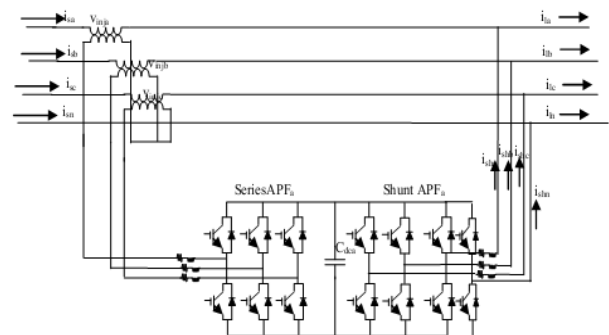


Fig. 4. 3P4W distribution system:

Recently, the utility service providers are putting more and more restrictions on current total harmonic distortion (THD) limits, drawn by nonlinear loads, to control the power distribution systems harmonic pollution. At the same time, the use of sophisticated equipment/load has increased significantly, and it needs clean power for its operation. Therefore, in future distribution systems and plant/load centers, application of UPQC would be common. The 3P4W topology that can be realized from 3P3W system This system has all the advantages of general UPQC, in addition to easy expansion of 3P3W system to 3P4W system.

Thus, this topology may play an important role in the future 3P4W distribution system for more advanced UPQC-based plant/load center installation, where utilities would be having an additional option to realize a 3P4W system just by providing a 3P3W supply. The UPQC should necessarily consist of three-phase series transformer in order to connect one of the inverters in the series with the line to function as a controlled voltage source. If we could use the neutral of three-phase series transformer to connect a neutral wire to realize the 3P4W system. 3P4W system can easily be achieved from a 3P3W system. The neutral current, present if any, would flow through this fourth wire toward transformer neutral point. This neutral current can be compensated by using a split capacitor topology or a four-leg voltage-source inverter (VSI) topology for a shunt inverter.

The four-leg VSI topology requires one additional leg as compared to the split capacitor because the split capacitor topology essentially needs two capacitors and an extra control loop to maintain a zero voltage error difference between both the capacitor voltages, resulting in a more complex control loop to maintain the dc bus voltage at constant level.

Table .1. System Parameters

System quantities	values
System Voltage	230V (line to neutral),50Hz
Feeder impedance	$Z_s= 1+j3.141$ ohm
Linear Load	$Z=40+j79.6$ ohm
Non-Linear load	3 phase full bridge rectifier load feeding a R-L load of 150 ohm-380 mH
Series interfacing transformer	1:1
PI controller gain	$K_p=6, K_i= 5.2$
Hysteresis band	$h1=+/- 0.5$ A, $h2=+/-6.9$ V

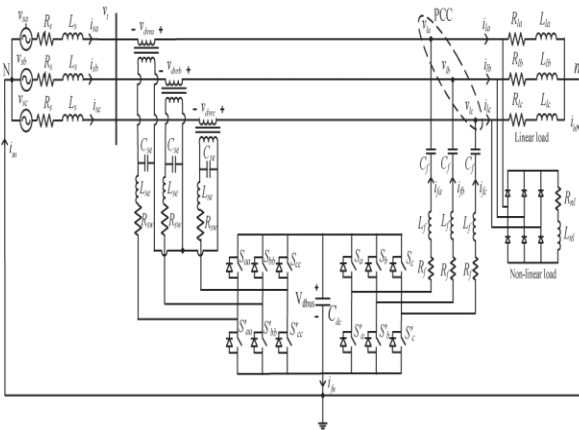
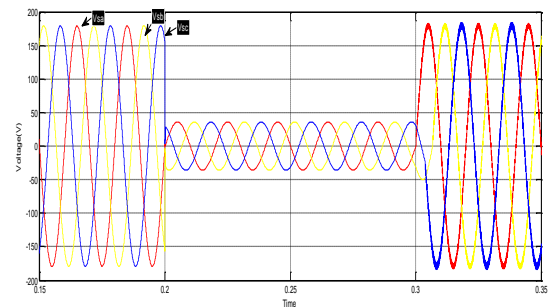


Fig. 5. 3P4W UPQC structure

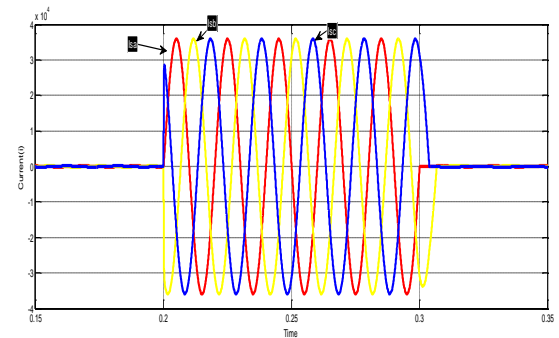
III.MATLAB/SIMULINK RESULTS

In order to validate the proposed topology, simulation is carried out using graphic-driven simulation software Matlab/Simulink R2013a. The same system parameters which are given Table I with additional  $C_f$  for a desired dc-link voltage are used to carry out simulation studies. The simulation results for both the conventional topology and the proposed modified topology are presented in this section for better understanding and comparison between both the topologies. The load currents and terminal (PCC) voltages before compensation are shown in

Fig.6.. The load currents are unbalanced and distorted as shown in Fig. 6(1), the terminal voltages are also unbalanced and distorted because these load currents.

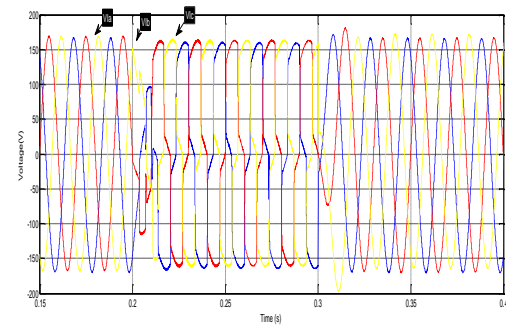


Time(sec) (1)

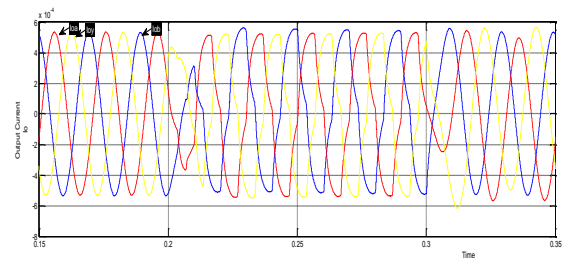


(2)Fig.6. Simulation results before compensation

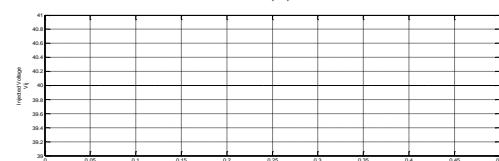
(1) Load Current (2) Terminal voltages



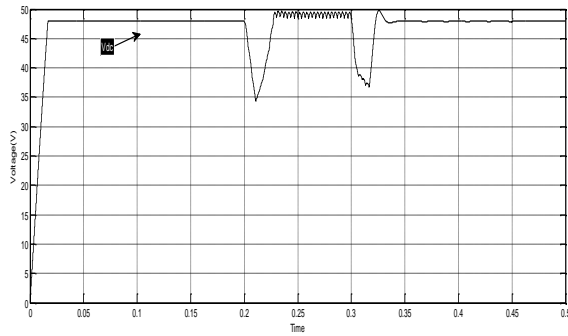
Time(sec) (1)



Time(sec) (2)



(3)



(4)  
Fig.7. Simulation result using UPQC topology (1) Terminal voltage after compensation (2) Source current after compensation (3) DC link voltage (4) DC capacitor voltage

One more advantage of having less voltage across the inductor is that the hysteresis band violation will be less. This will improve the quality of compensation, and total harmonic distortion (THD) reduces in the proposed topology.

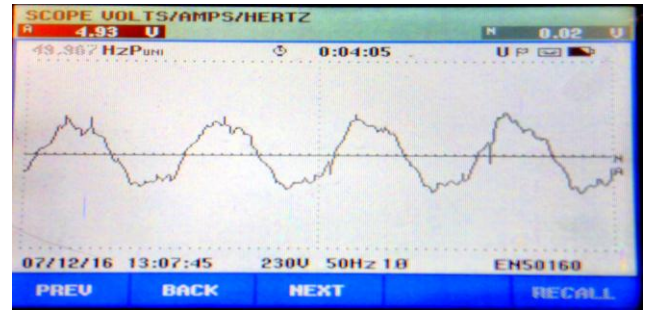
Table II. Source Current and Terminal Voltage Parameter

Source Current and Terminal Voltage Parameter	Without Compensation	With UPQC Topology.
isa	3.5	0.47
isb	3.7	0.50
isc	3.4	0.49
Vsa	40	185
Vsb	39	187
Vsc	40.5	183

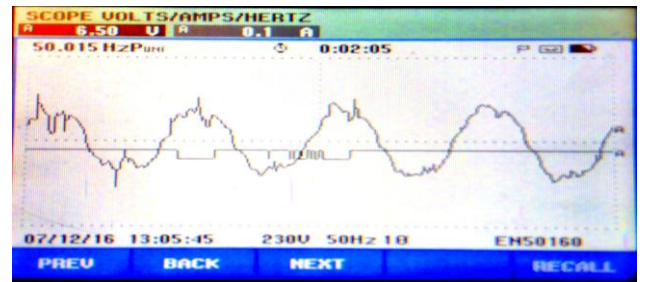
Similarly, the switching in the series active filter also reduces marginally as the dc-link voltage is reduced. The voltage Sag and Current swell of the load voltages and source currents before and after compensation in all the three-phases are shown in Fig.7. This clearly shows the modified topology performance is better than the conventional topology with a less dc-link voltage, reduction in switching operation, and regular tracking of reference compensator currents and which also verify through the Table II. Which elaborate the power quality problems in Source Current, terminal Voltage, harmonics. The source currents and load voltages before and after compensation in all the three-phases are given in Table II.

**IV. EXPERIMENTAL STUDIES**

The efficiency of the proposed scheme is verified with experimental studies. A prototype of the three-phase UPQC has been developed in the laboratory and result are verified using 435II series Power and Energy logger . The system parameters UPQC are the same as given in Table I, with the source voltage rms value of 100 V. The three-phase power quantities (voltages and currents) are converted to low-level voltage signals using Hall effect voltage and current transducers. In the experimental setup, the voltage is scaled down from 230 V ac range to 12 V ac range. These signals are further conditioned using isolation transformer having turns ratio of 1:1 and given to the further topology and result are obtained for phase ‘a’ for better understanding



(a)



(b)



(c)

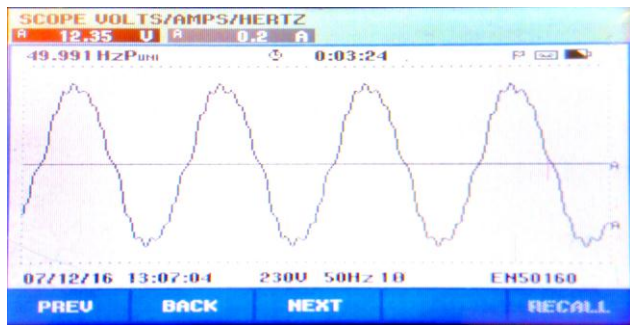
Fig.8.1..Experimental results. (a)Terminal voltages before compensation. (b) Load currents before compensation. (c) Total Harmonic distortion before compensation.

Use of

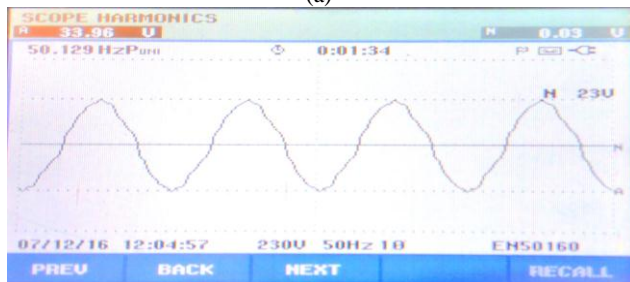
- 1) Microcontroller PIC 16F877A.
- 2) Opto-couplers.
- 3) Gate driver.
- 5) Three Phase PWM inverter (MOSFET).

In this project PIC microcontroller used as PWM circuit which produce PWM pulse at port B (pin PB 0 to PB 5).microcontroller has programmed to produce high pulse for either 3303 micro second or 30 micro second After this optocoupler IC MCT2E is connected between microcontroller or gate drive MCT2E has Gallium Arsenide diode which infrared frequency source and optically coupled with Silicon NPN phototransistor. MCT2E is used for electrical isolation between high and low power circuitry. As MOSFET transistor which has capacitive input for high speed switching. It operates on bootstrap principal. The gate charge for high side MOSFET is provided by the bootstrap capacitor which is charge by 12v supply through the bootstrap diode during the time when the devices are off since the capacitor is charged from the low voltage source to the power consumed by the drive. The output is connected to the gate of three phase inverter MOSFET.

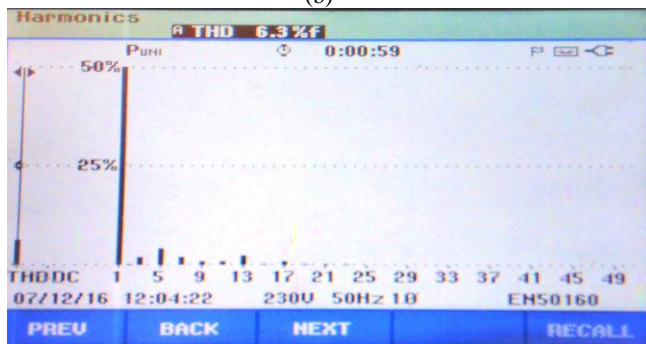




(a)



(b)



(c)

Fig 8.2. Experimental results using UPQC topology (a) Terminal voltages and Load currents after compensation.(b) Harmonic waveform after compensation. (c) THD after compensation. The three phase inverter consists of six MOSFET switches which are switching in the regular interval to generate the three phase. The figure clearly shows the simultaneous performance of the shunt and series active filter of the UPQC by compensating the load current and maintaining the load voltage to the desired value during voltage sag duration.

Table III. % THD of Source Current and Terminal Voltage.

Source Current and terminal Voltage	%THD
Without Compensation	14.7
With UPQC Topology	6.3
UPQC Theory	3.31-4.35

Thus, the average switching frequency of the switches in the proposed topology will be less as compared to conventional topology One more advantage of having less voltage across the inductor is that the hysteresis band violation will be less.

The THD comparison of the source currents and the terminal voltages before and after compensation with UPQC topology are given in Table III. This will improve the quality of compensation and THD will be less in the proposed topology. the average switching frequency of the shunt and series inverters with proposed topology has been reduced. The switching losses in the inverter has been calculated using the procedure From the

experimental results, the modified topology gives a reduced THD both in the source currents and terminal voltages with a reduced dc-link voltage along with reduction in average switching frequencies.

**V. CONCLUSION**

The proposed control scheme for three-phase, four-wire UPQC is validated and compared theory through the simulation results using MATLAB/Simulink R2013a software, and experimental results obtained using 435 II series Power and Energy Logger by development of a three phase 12V ac range prototype for obtaining result in laboratory. The performance of the UPQC is satisfactory in various power quality improvements, such as source current, Terminal Voltage mitigation, power-factor correction, voltage harmonics mitigation, and current harmonic mitigation. Supply currents and load voltage harmonic levels verified using both simulation as well as by experimental studies as shown in table II and III. under all conditions. The computational delay is reduced by indirectly controlling the three-phase supply currents/voltages.

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